KAMLESH MAHESHWARI

SHANTI, H.No. 110, 4th A-Cross, East of NGEF Layout,
Kasturi Nagar, Bangalore - 560043
Cell # +91-9008002839
E-mail : kamlesh.maheshwari@gmail.com

CAREER OBJECTIVE

To work in a dynamic organization so as to be able to use my skill set to the advantage of my organization and make strong contribution to organizational goals through continual development of professional skills. Would also like to grow with organization as a responsible member of the team.

Background SUMMARY

- A highly motivated, skilled professional with **close to 11 years** experience in VLSI Industry. Currently working with **TI, India as Lead Engineer**.
- Extensive front-end design experience. Worked on following roles and responsibilities :
  - Lead SoC Verification
  - SoC Functional Verification and Testbench Environment Setup
  - SoC Low Power Verification (CPF)
  - Tester Pattern verification environment setup and Functional Pattern Delivery for Tester
  - Formal Verification
  - IP Verification
  - SoC Validation
  - SoC Integration

PROFESSIONAL EXPERIENCE

Organization	Designation	Duration
Texas Instruments India Pvt. Ltd, Bangalore	Lead Engineer	May-12 to Present
FREESCALE, India Design center, Noida	Verification Lead	Jan 11 – Apr 12
FREESCALE, India Design center, Noida	Sr. Design Engineer	Dec 06 – Dec 10
FREESCALE, India Design center, Noida	Design Engineer	Apr 04 – Dec 06
MOTOROLA, India design center, Noida	Design Engineer	July 03 – Apr 04

EDUCATION SUMMARY

Qualification	University/Board	Result	Year
B.Tech (EcE)	IT-BHU	7.48 (DGPA)	2003
XII	Board of Secondary Education, Rajasthan	81.53%	1998
X	Board of Secondary Education, Rajasthan	86%	1996

TECHNICAL SKILLS

- Programming Languages**:**
  - **Verilog**
  - **System Verilog**
  - **C**
  - **Perl**
  - **ARM processor assembly**
  - **Power PC assembly**

- Operating Systems**:**
  - **UNIX**
  - **Windows**
  - **Linux**

- Tools:
  - **Cadence**: IUS, IFV,CPF
  - **Synopsis**: VCS
  - **Novas**: Debussy
  - **Sequence:** Power Theater
  - **Freescale**: Rabbit, Viper, SVBCL

- **Project Summary**

Company	Texas Instruments India Pvt. Ltd.
Project	C65 Safety IC
Period	July 2013 : Present
Description	Arm Cortex R4 (Lockstep Architecture) based SoC for Safety Application.
Responsibilities	• **Responsible for verification of DCAN, ADM, DEBUG and DEVICE category.** • **Regression Environment Setup** • **Mixed Signal Verification for ADC, LPO, GF and Reset Seq.** • **GLS Closure DCAN, ADM, DEBUG, DEVICE and GCM category**
Methodology	• **TDL reduction proposal based on Coverage.**

Company	Texas Instruments India Pvt. Ltd.
Project	C65 Safety IC
Period	Feb 2013 : July 2013
Description	Arm Cortex R4 (Lockstep Architecture) based SoC for Safety Application.
Responsibilities	• **TDL closure for TMS of multiple device.**

Company	Texas Instruments India Pvt. Ltd.
Project	C65 Safety IC
Period	May 2012 : Jan 2013
Description	Arm Cortex R5 (Lockstep Architecture) based SoC for Safety Application.
Responsibilities	• **GLS closure for EMIF, I2C, VIM modules.** • **TDL generation for multiple modules.** • **TDL reduction proposals** • **Char pattern reduction analysis and proposal for EMIF Async (Slow – Fast Interface)**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CMOS90 Auto IC
Period	July 2011 : Apr:2012
Description	Dual Core Architecture with ARM Cortex A5 and M4 based processors for Infotainment, Cluster as well as high end industrial and general purpose applications.
Responsibilities	• **Lead Clock and Reset Module Verification team** • **Responsible for Verification of Low Power Architecture** • **IFV environment for Clock connectivity including clocking gating logic**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CMOS90 Auto IC
Period	Nov 2010 : Jun 2011
Description	Power PC Architecture based microcontrollers that target automotive vehicle body and gateway applications. This product was a derivative product with some changes.
Responsibilities	• **Lead Verification team (includes 5 verification engineer) for the SoC Verification. Team was having 4 new engineers** • **Validate software compatibility with previous SoC for the changes.** • **Tester Environment Setup and Pattern Delivery : Developed tester environment , Wrote Functional and Exposed pattern for Analog modules. Work with TE team for debugging failures**
Awards	**Bravo for the activities**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CMOS90 Auto IC
Period	Apr 2009 : Oct 2010
Description	Power PC Architecture based microcontrollers that target automotive vehicle body and gateway applications. This product was having Dual Cores.
Responsibilities	• **SoC Functional Verification Environment and Testbench Development : Integrate PIN Drivers, Write Clock and Reset Drivers, C-API Environment, C-Verilog Micro Operating System Development.** • **Independent Verification Environment for Individual Cores and Envioronment for Dual Core as well** • **Formal Verification : Used IFV for testing of multiplexing logic like the IOMUX** • **SIUL and STCU Verification : Verification of System Integration Unit and Functional MBIST Module. Developed Perl script to generate pattern to verifiy IOs.** • **Tester Environment Setup and Pattern Delivery : Developed tester environment , Wrote Functional and Exposed pattern for Analog modules. Work with TE team for debugging failures** • **CPF environment setup** • **GLS Environment setup and verification**
Awards	• **Bravo for verification environment and tester activities.**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CCM/SRC IP Verification
Period	Sep 2007 : Mar 2009
Description	CCM (Clock Controller module) controls uses the available clock sources and generates the clocks for SoC. CCM also manages clock gating and low power modes. SRC (System Reset Controller) controls the Reset and Boot mode operation of the SOC.
Responsibilities	• **Developed Random Verification Environment to program and check clock generation** • **Developed SV-assertion for Low Power sequences, Reset Generation** • **Verification of clock generation, clock dividers, glitchless muxing** • **Low Power handshaking verification** • **Verification of Various Reset generation**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CMOS65 Baseband IC
Period	Apr 2006 : Aug 2007
Description	This SoC has Dual Processor (MXC) Architecture. It provides the baseband (modem) and application processor functions for UMTS.
Responsibilities	• **IOMUX/Padring generation and integration : Implemented Tcl/Perl based scripts for IOMUX/IOMUXC/PADRING generation. Developed PERL scripts to run on PINMUXING and then used RABBIT and VIPER to generate IOMUX Verilog and PADRING Verilog and PADRING def. Also delivered Integration scripts.** • **Post Silicon Validation on Evaluation Board : Was responsible for Validating Low Power Modes (Power Gating), SPI , SSI modules**
Awards	**Received Bravo for IOMUX/PADRING activiteis.** **Special Recogntion by PI team for PADRING Integration**

Company	Freescale Semiconductor India Pvt. Ltd.
Project	CMOS90 Baseband IC
Period	Apr 2005 : Mar 2006
Description	This SoC has Dual Processor design containing Starcore which takes up the role of processing all the modem functions on the baseband and an ARM9 core which takes up the role of processing all the Application Processor functions.
Responsibilities	• **System Level Power Analysis : Setup environment for Low power mode power analysis at RTL and Gate level Netlist. Report Clock Tree and Overall power.** • **IOMUX/Padring generation and integration : Implemented Tcl/Perl based scripts for IOMUX/IOMUXC/PADRING generation. Developed PERL scripts to run on PINMUXING and then used RABBIT and VIPER to generate IOMUX Verilog and PADRING Verilog and PADRING def. Also delivered Integration scripts.** • **Post Silicon Validation on Evaluation Board : Was responsible for Validating Low Power Modes, SPI , SSI modules**

Company	Motorola India Pvt. Ltd/ Freescale Semiconductor India Pvt. Ltd.
Project	CMOS90 Baseband IC
Period	Oct 2003 : Mar 2005
Description	This SoC has Dual Processor design containing Starcore which takes up the role of processing all the modem functions on the baseband and an ARM11 core which takes up the role of processing all the Application Processor functions.
Responsibilities	• **SoC Memory Map Verification : Writing patterns to verify system level memory map** • **Front End integration : Toplevel integration of the IC and deliver netlist Environment to Verification and Synthesis team** • **SoC Functional Verification Environment and Testbench Development : Integrate Drivers, Write Clock and Reset Drivers, C-API Environment, C-Verilog Micro Operating System Development** • **Tester Environment Setup and Pattern Delivery : Developed tester environment , Wrote Functional and Characterization Patterns**
Awards	**Received BRAVO for various activities**